ABSTRACT OF THE DISCLOSURE

A semiconductor memory apparatus that stores data by accumulating charges in its capacitor is provided for allowing itself to be operated at a low potential and at a high speed. In the semiconductor memory apparatus, before performing a precharge by a precharging circuit 10 for the next cycle of read and write, a forced step-down circuit 11 previously lowers the potential of the bit line BL charged on the high side to a level within the range of preventing data of positive charges written and stored in a memory cell MC from being disappeared.